COMMENTS

The enclosed is responsive to the Examiner's Final Office Action mailed on February 6, 2002. At the time the Examiner mailed the Final Office Action, claims 1 -62 were pending. In response, pursuant to a "file wrapper" continuation (under CFR 1.53(d)) which is filed herewith, the Applicant has: 1) amended claims 1-3, 8-10, 54-62; and, 2) added new claims 63 through 87. No claims have been canceled. As such, claims 1-87 are currently pending. The Applicant respectfully requests reconsideration of the present application and the allowance of claims 1-87.

The Examiner has rejected independent claims 1, 24, 41 and 54 under 35 USC 102(b) as being anticipated by US Patent No. 5,436,955 (hereinafter, "Kaewell"). To anticipate a claim, the reference must teach every element of the claim, MPEP 2131. The applicant respectfully submits that: 1) the element "*continuously broadcasting* a plurality of firmware algorithms" in independent claim 1 is not disclosed by Kaewell; 2) the element "at least one channel over which a plurality of firmware algorithms are *continuously broadcasted*" in independent claim 25 is not disclosed by Kaewell; 3) the element "the serial bus comprising a plurality of channels over which a plurality of firmware algorithms are *continuously broadcasted*" in claim 41 is not disclosed by Kaewell; and, 4) the element "selectively monitoring for and receiving at least one firmware algorithm from amongst a plurality of *continuously broadcasted* firmware algorithms" of claim 54 is not disclosed by Kaewell. As such, it is the Applicant's position that independent claims 1, 24, 41 and 54 are patentable over Kaewell.

The Examiner cited from Kaewell each of column 2, line 65 to column 3, line 1; column 3, lines 9-29; column 4, lines 28-30; and column 4 lines 53-68 as disclosing the continual broadcasting of firmware. See, the Examiner's Final Office Action, pg. 2. An examination and discussion of each of these sections of Kaewell is provided immediately below.

Sections of Kaewell Cited By the Examiner As Basis For Rejecting The Applicant's Claims

Column 2, line 65 to Column 3, line 1 of Kaewell provides:

> The effective sampling rate of the digital cellular system equipment is 48.6 k-samples/sec. and, therefore the 8 k-sample/sec processed speech signal has to be interpolated up to the 48.6 k-sample/sec. rate.

Column 3, lines 9 - 29 of Kaewell provides:

> Fig. **2** shows the basic components of a single analog channel unit at a cell site base station. The hardware comprises a Modulator/Downconverter Module (MDM) **9** and a Slot Processing Module (SPM) **10**. The MDM **9** is connected to receiving and transmitting antennaes and performs all the RF and IF processing, while the SPM **10** performs all the baseband processing for the channel unit. Two receiving antennaes A and B are shown providing input signals to the MDM **9**, these being for a space diversity reception system, and the MDM **9** provides an output signal to a single transmitting antennae. Although not shown in Fig. **2**, the SPM **10** can accommodate two MDMs **9**, supporting up to two transmitting channels and four receiving channels.

Column 4, lines 28-30 of Kaewell provides:

> The resulting output from these processes is stored in the DPRAMs to be fetched by the Tx_DSP **15**.

The three above quoted portions of Kaewell simply do not relate to the manner in which firmware is obtained by a DSP. The first quotation (column 2, line 65 to column 3, line 1) simply discusses the data rate of a voice channel. The second quotation (column 3, lines 9-29) simply states that a cell phone base

station is comprised of a wireless modulation/demodulation unit (MDM) and a signal processing unit (SPM). The third quotation (column 4, lines 28-30) states that the output values of DSP are stored in a memory. Throughout either of these quotations, the word "firmware" is not used; and, the manner in which a DSP's firmware is obtained by a DSP is not discussed. As such, it is impossible for column 2, line 65 to column 3, line 1 of Kaewell; column 3, lines 9-29 of Kaewell; or, column 4, lines 28-30 of Kaewell to disclose or even suggest the continual broadcasting of firmware to a DSP. Thus, use of these sections of Kaewell as a basis for rejecting the Applicant's claims with respect to their claiming the continual broadcasting of firmware to a DSP is improper; and, likewise, the Applicant's claims are patentable over these sections of Kaewell.

Column 4 lines 53-68 of Kaewell provides:

> The receive signal is processed by the Rx_DSPs **11** and **12** under the control of the analog firmware to perform the functions of sampling gate combiner **52**. The sampling gate combiner function **52** performs a sampling rate conversion of the 48.6 k-sample/sec. rate to 40.0 k-samples/-sec. to give four samples per FSK symbol and to allow the eventual integer decimation of the speech signals down to the 8 k-sample/sec. PCM (pulse code modulation) rate for interfacing to the T1 transmission system. The speech signals are then further processed, again by the Rx DSPs **11** and **12** under the control of the analog firmware, in voice processing functions **53**. Voice processing function **53** performs the decimation of the speech signals to the T1 lines via the SPDF.

The above quoted portion of Kaewell, again, simply does not relate to the manner in which firmware is obtained by a DSP. The above quotation discloses, at most, that different functions may be performed by a DSP with firmware (e.g., a gate combiner function and a voice processing function). Better said, this portion of Kaewell relates more to how firmware is used rather than to how it is obtained. As such, it is impossible for column 4 lines 53-68 of Kaewell to disclose or even suggest the continual broadcasting of firmware to a DSP. Thus,

use of this section of Kaewell as a basis for rejecting the Applicant's claims with respect to their claiming the continual broadcasting of firmware to a DSP is improper; and, likewise, the Applicant's claims are patentable over this section of Kaewell.

Other Portions of Kawell Not Cited By the Examiner

The only section of Kaewell that addresses the manner in which firmware is obtained by a DSP is found in column 4, lines 4-21 which is provided below (emphasis added):

> To operate as an analog channel unit, *the controller 16 must load the analog firmware into the five DSPs **11**, **12**, **13**, **14** and **15** and then send configuration commands to each DSP specifying its mode of operation (e.g., traffic channel, control channel). Once the firmware has been loaded, the DSPs respond to the configuration command by executing the modules needed to operate in the configured mode*. This is accomplished according to the invention providing the static RAMs (SRAMs) **41**, **42**, **43**, **44** and **45** for each of the DSPs **11**, **12**, **13**, **14**, and **15**. More specifically, the firmware is downloaded via the SPDF interface **32**, arbiter logic **31**, bus **30** and DPRAMs **26**, **27**, **28** and **20** to the SRAMs **41**, **42**, **43**, and **44** and via the SPDF interface **32** and arbiter logic **31** directly to the SRAM **45**. This firmware can later be replaced by firmware that reconfigures the system to operate in a purely digital fashion.

The above quoted portion of Kaewell fails to disclose or suggest the continual broadcasting of firmware. Instead, the underlined portion of the above quotation suggests that DSPs are initially provided a complete copy of their firmware (e.g., at system power on); and, then, the DSPs execute the initially supplied firmware so as to perform a larger function (e.g., traffic channel, control channel) as specified by controller 16. Better said, Kaewell suggests an initial downloading of all the firmware the DSP "may" use over its lifetime rather than a "continual broadcasting" of smaller units of firmware to a DSP over the course of its lifetime. In the later approach, to which the Applicant's specification is directed, a DSP can continually pick and choose (e.g., as needed) smaller

pieces of firmware (e.g., wherein newly selected firmware replaces previously selected firmware in the DSP's memory) over the course of its lifetime because the smaller pieces of firmware are being continually broadcasted to the DSP.

Thus, when firmware is continually broadcasted, a DSP that receives the broadcast is continually supplied with whatever firmware is appropriate for the particular function the DSP is to next perform. As such, as just one example, the DSP may be implemented with less memory because it can continually overwrite "stale" firmware (used to perform a prior function) with "new" firmware (used to perform its next function). In order to further emphasize this perspective, the Examiner's attention is drawn to page 9, lines 1-20; page 12, lines 1-14; page 12, line 24 to page 13, line 3; page 15, lines 6-17; page 15, line 26 to page 16, line 23 of the Applicant's specification. As such, in summary, independent claims 1, 24, 41 and 54 are patentable over Kaewell because Kaewell does not disclose or suggest the continual broadcasting of firmware to a DSP. As such each of claims 1-62 are patentable over Kaewell. Also, new independent claims 68, 83, 86 and 87 are also patentable over Kaewell for similar reasons.

The Applicant respectfully requests reconsideration of the present application and the allowance of claims 1 through 87.

If there are any additional charges, please charge Deposit Account No. 02-2666.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

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Robert B. O'Rourke
Reg. No. 46,972

12400 Wilshire Blvd.
Seventh Floor
Los Angeles, CA 90025-1026
(408) 720-8300

CLAIMS SHOWING AMENDMENTS

Please replace claims 1-3, 8-10, 54-62 with the following claims:

1. (Amended) A method for supporting digital signal processing (DSP) of a plurality of data types, the method comprising [the steps of]:

continuously broadcasting a plurality of firmware algorithms to a plurality of DSP engines over a channelized serial bus; and

selectively monitoring for and receiving at least one firmware algorithm of the plurality of firmware algorithms by at least one of the plurality of DSP engines, wherein the at least one firmware algorithm is used to process data of at least one corresponding data type received by the at least one of the plurality of DSP engines over at least one data line.

2. (Amended) The method of claim 1, further comprising [the steps of]:

receiving at least one pulse coded modulation (PCM) data stream from a public switched telephone network (PSTN);

generating at least one packet of data from the PCM data stream using the received at least one firmware algorithm; and

transmitting the at least one packet of data over an Internet Protocol (IP) network.

3. (Amended) The method of claim 1, further comprising [the steps of]:

receiving at least one packet of data from an IP network;

generating at least one PCM data stream from the at least one packet of data using the at least one firmware algorithm; and

transmitting the at least one PCM data stream over a PSTN.

4. (Unchanged) The method of claim 1, wherein the at least one data line comprises at least one bidirectional PCM data stream.

5. (Unchanged) The method of claim 1, wherein the at least one data line comprises at least one bidirectional host bus.

6. (Unchanged) The method of claim 1, wherein the plurality of firmware algorithms are continuously broadcasted to a plurality of service DSP engines by a master DSP engine resident in a processor.

7. (Unchanged) The method of claim 6, wherein the channelized serial bus comprises eight channels.

8. (Amended) The method of claim 7, wherein the [step of] selectively monitoring for and receiving at least one firmware algorithm comprises [the steps of]:

determining a data type of the data received into at least one of the plurality of service DSP engines;

determining at least one firmware algorithm required to process the received data;

determining an address of at least one channel of the serial bus on which the required at least one firmware algorithm is available.

9. (Amended) The method of claim 8, wherein the [step of]selectively monitoring for and receiving at least one firmware algorithm further comprises [the step of] unmasking a bit of an interrupt mask in the at least one of the plurality of service DSP engines, the unmasked bit corresponding to the address of at least one channel of the serial bus on which the required at least one firmware algorithm is transmitted.

10. (Amended) The method of claim 9, wherein the [step of] selectively monitoring for and receiving at least one firmware algorithm further comprises [the steps of]:

executing at least one interrupt service routine in response to receiving an interrupt signal corresponding to the unmasked interrupt bit;

receiving the at least one firmware algorithm in response to execution of the interrupt service routine; and

storing the received at least one firmware algorithm in a memory of the service DSP.

11. (Unchanged) The method of claim 8, wherein each service DSP memory comprises data correlating each of the plurality of firmware algorithms with a serial bus channel on which each of the plurality of firmware algorithms are transmitted.

12. (Unchanged) The method of claim 8, wherein the data correlating each of the plurality of firmware algorithms with a serial bus channel on which each of the plurality of firmware algorithms are transmitted is downloaded to each service DSP engine from the processor.

13. (Unchanged) The method of claim 8, wherein the data correlating each of the plurality of firmware algorithms with a serial bus channel on which each of the plurality of firmware algorithms are transmitted is hard-coded in each of the service DSP engines.

14. (Unchanged) The method of claim 7, wherein each channel of the channelized serial bus transmits at least one firmware algorithm.

15. (Unchanged) The method of claim 6, wherein the plurality of firmware algorithms are stored in a memory of the master DSP engine.

16. (Unchanged) The method of claim 1, wherein the continuous broadcast is repetitive.

17. (Unchanged) The method of claim 1, wherein the plurality of data types comprise modem data, voice data, audio data, video data, and facsimile data.

18. (Unchanged) The method of claim 1, wherein each DSP engine comprises at least one channel.

19. (Unchanged) The method of claim 7, wherein at least one algorithm is transmitted on a channel of the channelized serial bus.

20. (Unchanged) The method of claim 7, wherein an algorithm is transmitted using at least one channel of the channelized serial bus.

21. (Unchanged) The method of claim 1, wherein each of the plurality of DSP engines comprise a memory for storing the at least one firmware algorithm.

22. (Unchanged) The method of claim 1, wherein each of the plurality of firmware algorithms are broadcasted using at least one serial block, wherein each of the broadcasted at least one serial blocks comprise a portion of each of the plurality of firmware algorithms.

23. (Unchanged) The method of claim 22, wherein the at least one serial block comprises 1024 information bits.

24. (Unchanged) The method of claim 22, wherein the broadcast of each of the at least one serial blocks is preceded by a broadcast of an address signal, the address signal identifying the firmware algorithm of the broadcasted at least one serial block.

25. (Unchanged) An apparatus for supporting digital signal processing (DSP) of a plurality of data types, the apparatus comprising:

a serial bus comprising at least one channel over which a plurality of firmware algorithms are continuously broadcasted; and

a plurality of DSP engines coupled to the serial bus and to at least one data line, at least one of the plurality of DSP engines selectively monitoring for and receiving at least one firmware algorithm of the plurality of firmware algorithms broadcasted, wherein the at least one firmware algorithm is used to process data received by the at least one of the plurality of DSP engines over the at least one data line.

26. (Unchanged) The apparatus of claim 25, further comprising a master DSP engine resident in a host processor, the master DSP engine coupled to the serial bus, wherein the master DSP engine continuously broadcasts the plurality of firmware algorithms to a plurality of service DSP engines.

27. (Unchanged) The apparatus of claim 26, wherein:

at least one pulse coded modulation (PCM) data stream is received from a public switched telephone network (PSTN);

at least one packet of data is generated from the PCM data stream using the received at least one firmware algorithm; and

the at least one packet of data is transmitted over an Internet Protocol (IP) network.

28. (Unchanged) The apparatus of claim 26, wherein:

at least one packet of data is received from an IP network;

at least one PCM data stream is generated from the at least one packet of data using the at least one firmware algorithm; and

the at least one PCM data stream is transmitted over a PSTN.

29. (Unchanged) The apparatus of claim 25, wherein the at least one data line comprises at least one bidirectional PCM data stream.

30. (Unchanged) The apparatus of claim 25, wherein the at least one data line comprises at least one bidirectional host bus.

31. (Unchanged) The apparatus of claim 26, wherein the plurality of service DSP engines selectively monitor for and receive the at least one firmware algorithm by:

determining a data type of the data received into at least one of the plurality of service DSP engines;

determining at least one firmware algorithm required to process the received data;

determining an address of at least one channel of the serial bus on which the required at least one firmware algorithm is available.

32. (Unchanged) The apparatus of claim 31, wherein the plurality of service DSP engines selectively monitor for and receive the at least one firmware algorithm by unmasking a bit of an interrupt mask in the at least one of the plurality of service DSP engines, the unmasked bit corresponding to the address of at least one channel of the serial bus on which the required at least one firmware algorithm is transmitted.

33. (Unchanged) The apparatus of claim 32, wherein the plurality of service DSP engines selectively monitor for and receive the at least one firmware algorithm by:

executing at least one interrupt service routine in response to receiving an interrupt signal corresponding to the unmasked interrupt bit;

receiving the at least one firmware algorithm in response to execution of the interrupt service routine; and

storing the received at least one firmware algorithm in a memory of the service DSP.

34. (Unchanged) The apparatus of claim 31, wherein the data correlating each of the plurality of firmware algorithms with a serial bus channel on which each of the plurality of firmware algorithms are transmitted is downloaded to each service DSP engine from the host processor.

35. (Unchanged) The apparatus of claim 25, wherein the data received by the at least one of the plurality of DSP engines comprises at least one channel of multiplexed data received over a public switched telephone network, the data having at least one of the plurality of data types.

36. (Unchanged) The apparatus of claim 25, wherein the plurality of data types comprise modem data, voice data, audio data, and facsimile data.

37. (Unchanged) The apparatus of claim 25, wherein each DSP engine comprises at least one channel.

38. (Unchanged) The apparatus of claim 26, wherein at least one algorithm is transmitted on a channel of the channelized serial bus.

39. (Unchanged) The apparatus of claim 26, wherein an algorithm is transmitted using at least one channel of the channelized serial bus.

40. (Unchanged) The apparatus of claim 25, wherein each of the plurality of firmware algorithms are broadcasted using at least one serial block, wherein each of the broadcasted at least one serial blocks comprise a portion of each of the plurality of firmware algorithms, wherein the portion of each of each of the plurality of firmware algorithms comprises 1024 information bits.

41. (Unchanged) A multiservice digital signal processing (DSP) system comprising:

a processor coupled to at least one data line, the processor comprising a master DSP engine, wherein the at least one data line provides a plurality of data types;

a serial bus coupled to the master DSP engine, the serial bus comprising a plurality of channels over which a plurality of firmware algorithms are continuously broadcasted; and

a plurality of service DSP engines coupled to the at least one data line and the serial bus, at least one of the plurality of service DSP engines selectively monitoring for and receiving at least one firmware algorithm over the serial bus, wherein the at least one firmware algorithm is used to process data of at least one corresponding data type received by the at least one of the plurality of service DSP engines over the at least one data line.

42. (Unchanged) The system of claim 41, wherein:

at least one pulse coded modulation (PCM) data stream is received from a public switched telephone network (PSTN);

at least one packet of data is generated from the PCM data stream using the received at least one firmware algorithm; and

the at least one packet of data is transmitted over an Internet Protocol (IP) network.

43. (Unchanged) The system of claim 41, wherein:

at least one packet of data is received from an IP network;

at least one PCM data stream is generated from the at least one packet of data using the at least one firmware algorithm; and

the at least one PCM data stream is transmitted over a PSTN.

44. (Unchanged) The system of claim 41, wherein the at least one data line comprises at least one bidirectional PCM data stream.

45. (Unchanged) The system of claim 41, wherein the at least one data line comprises at least one bidirectional host bus.

46. (Unchanged) The system of claim 41, wherein the plurality of service DSP engines selectively monitor for and receive the at least one firmware algorithm by:

determining a data type of the data received into at least one of the plurality of service DSP engines and determining at least one firmware algorithm required to process the data type;

determining an address of at least one channel of the serial bus on which the required at least one firmware algorithm is available; and

unmasking a bit of an interrupt mask in the at least one of the plurality of service DSP engines, the unmasked bit corresponding to the address of at least one channel of the serial bus on which the required at least one firmware algorithm is transmitted.

47. (Unchanged) The system of claim 46, wherein the plurality of service DSP engines selectively monitor for and receive the at least one firmware algorithm by:

executing at least one interrupt service routine in response to receiving an interrupt signal corresponding to the unmasked interrupt bit;

receiving the at least one firmware algorithm in response to execution of the interrupt service routine; and

storing the received at least one firmware algorithm in a memory of the service DSP.

48. (Unchanged) The system of claim 46, wherein the data correlating each of the plurality of firmware algorithms with a serial bus channel on which each of the plurality of firmware algorithms are transmitted is downloaded to each service DSP engine from the processor.

49. (Unchanged) The system of claim 41, wherein the data received by the at least one of the plurality of DSP engines comprises at least one channel of multiplexed data received over a public switched telephone network, the data having at least one of the plurality of data types comprising modem data, voice data, audio data, and facsimile data.

50. (Unchanged) The system of claim 41, wherein each service DSP engine comprises at least one channel.

51. (Unchanged) The system of claim 41, wherein at least one algorithm is transmitted on a channel of the serial bus.

52. (Unchanged) The system of claim 41, wherein an algorithm is transmitted using at least one channel of the serial bus.

53. (Unchanged) The system of claim 41, wherein each of the plurality of firmware algorithms are broadcasted using at least one serial block, wherein each of the broadcasted at least one serial blocks comprise a portion of each of the plurality of firmware algorithms.

54. (Amended) A computer readable medium containing executable instructions which, when executed [in a processing system]by a digital signal processor (DSP), cause[s] the [system to perform digital signal processing (DSP) of a plurality of data types]DSP to perform a method, the method comprising:

[continuously broadcasting a plurality of firmware algorithms to a plurality of DSP engines over a channelized serial bus; and]

selectively monitoring for and receiving at least one firmware algorithm [of the]from amongst a plurality of continuously broadcasted firmware algorithms [by at least one of the plurality of DSP engines, wherein the at least one firmware algorithm is used to process data of at least one corresponding data type

received by the at least one of the plurality of DSP engines over at least one data line.]; and

processing data that has been received from a network with the at least one firmware algorithm.

55. (Amended) The computer readable medium of claim 54, [further causing the system to perform]wherein the processing further comprises[:

receiving at least one pulse coded modulation (PCM) data stream from a public switched telephone network (PSTN); and]

generating at least one packet of data from [the]a PCM data stream, the PCM data stream corresponding to the data that has been received from a network[using the received at least one firmware algorithm; and

transmitting the at least one packet of data over an Internet Protocol (IP) network].

56. (Amended) The computer readable medium of claim [54]55, [further comprising]wherein the network is a PSTN network[:

receiving at least one packet of data from an IP network;

generating at least one PCM data stream from the at least one packet of data using the at least one firmware algorithm, the packet of data having been received from an IP network; and

transmitting the at least one PCM data stream over a PSTN].

57. (Amended) The computer readable medium of claim 54, wherein the data that has been received from a network further comprises audio data[system is caused to continuously broadcast the plurality of firmware algorithms to a plurality of service DSP engines by a master DSP engine resident in a processor].

58. (Amended) The computer readable medium of claim 57, wherein selectively monitoring for and receiving at least one firmware algorithm comprises:

determining a data type of the data that has been received from a network[into at least one of the plurality of service DSP engines];

determining at least one firmware algorithm required to process the [received] data that has been received from a network;

determining an address of at least one channel of [the]a serial bus on which the required at least one firmware algorithm is available.

59. (Amended) The computer readable medium of claim 58, wherein selectively monitoring for and receiving at least one firmware algorithm further comprises unmasking a bit of an interrupt mask [in the at least one of the plurality of service DSP engines], the unmasked bit corresponding to the address of at least one channel of the serial bus on which the required at least one firmware algorithm is transmitted.

60. (Amended) The computer readable medium of claim 59, wherein selectively monitoring for and receiving at least one firmware algorithm further comprises:

executing at least one interrupt service routine in response to receiving an interrupt signal corresponding to the unmasked interrupt bit;

receiving the at least one firmware algorithm in response to execution of the interrupt service routine; and

storing the received at least one firmware algorithm in a memory [of the service DSP].

61. (Amended) The computer readable medium of claim 54, wherein the [processor is further configured so that data received by the at least one of the plurality of DSP engines comprises at least one channel of multiplexed data received over a public switched telephone network, the data comprising modem

data, voice data, audio data, and facsimile data]data that has been received from a network further comprises voice data.

62. (Amended) The computer readable medium of claim 54, wherein the data has been received from a network further comprises facsimile data[each of the plurality of firmware algorithms are broadcasted using at least one serial block, wherein each of the broadcasted at least one serial blocks comprise a portion of each of the plurality of firmware algorithms, wherein the broadcast of each of the at least one serial blocks is preceded by a broadcast of an address signal identifying the firmware algorithm of the broadcasted at least one serial block].